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09/903,178	07/11/2001	Hans-Peter Heigl	SC0897EM	9364

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2112	3

Jim Cligan
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Austin Intellectual Property Law Section
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DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,178	HEIGL ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(e) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(f) BRIEF SUMMARY OF THE INVENTION.
(g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(h) DETAILED DESCRIPTION OF THE INVENTION.
(i) CLAIM OR CLAIMS (commencing on a separate sheet).
(j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

1. In this case, the Applicants do not include (f) BRIEF SUMMARY OF THE INVENTION in the disclosure, which furnishes with the preferred layout for the specification of a utility application.

2. The disclosure is objected to because of the following informalities:

Substitute "Communication controller 10" in line 22 and in lines 29-30 for --Communication controller 20--. Appropriate correction is required.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "16" and "18" have both been used to designate channel handler in Fig. 1A. A proposed drawing correction or corrected drawings are required in reply to the Office Action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 2, 6-8, 11-16 and 18-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Yeivin et al. [WO 00/60477; cited by the Applicants; hereinafter Yeivin].

Referring to claims 1 and 11, Yeivin discloses a communication controller, which is a microcontroller unit (i.e., communication controller as indicated by dashed line 119 in Fig. 3), for communication on at least one communication bus (i.e., communication channels 180 in Fig. 3), each communication bus (i.e., communication channel) transferring a data stream (i.e., high speed data stream) according to a communication protocol (See page 7, lines 20-22), said communication controller comprising a communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) coupled to said at least one communication bus adapted to be programmable to perform transformations of said data stream (See page 10, lines 3-23).

Referring to claim 2, Yeivin teaches said communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) comprises a programmable decoder and/or encoder (i.e., first processor; See page 10, lines 3-23).

Referring to claim 6, Yeivin teaches said communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) is adapted to be programmable to perform transformations (See page 10, lines 3-23) of said data stream (i.e., high speed data stream) on bit-level (i.e., raw bit data stream; See page 9, line 31 through page 10, line 2).

Referring to claim 7, Yeivin teaches a communication control unit (i.e., second processor 100 of Fig. 3) for controlling (e.g., initializing) said communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3; See page 10, lines 24-28).

Referring to claim 8, Yeivin teaches a memory (i.e., instruction memory bank 130 or first memory bank 70 in Fig. 3) for storing instructions (See page 10, lines 3-9) to perform transformations of said data stream (i.e., high speed data stream) according to several communication protocols (See page 7, lines 20-22).

Referring to claim 12, Yeivin teaches said microcontroller unit (i.e., communication controller as indicated by dashed line 119 in Fig. 3) adapted to communicate on several communication buses simultaneously (i.e., communication channels 182 in Fig. 3), each communication bus transferring a data stream (i.e., high speed data stream) according to a respective communication protocol (See page 7, lines 20-22).

Referring to claim 13, Yeivin discloses a method (See Abstract) of using a communication controller (i.e., communication controller as indicated by dashed line 119 in Fig. 3) for communication on at least one communication bus (i.e., communication channels 180 in Fig. 3), each communication bus (i.e., communication channel) transferring a data stream (i.e., high speed data stream) according to a communication protocol (See page 7, lines 20-22), said communication controller comprising a communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) coupled to said at least one communication bus adapted to be programmable to perform transformations of said data stream (See page 10, lines 3-23), the method comprising the steps of selecting a communication protocol

(See page 9, line 11 through page 10, line 2, page 16, lines 21-27, and page 17, line 15-27; i.e., wherein in fact that a state machine of the peripheral being tailored to handle a communication protocol, and a request selector of the scheduler selecting RC(c) request channel anticipates selecting a communication protocol); programming said communication handler (i.e., first processor) with instructions to perform transformations of said data stream according to said selected communication protocol (See page 10, lines 3-23, and page 10, line 29 through page 11, line 25); receiving electrical signals (i.e., receiving raw data bit stream) representing data of said data stream (See page 9, line 19 through page 10, line 2); transforming (i.e., converting and processing) said electrical signals representing data of said stream by said communication handler (i.e., peripherals, scheduler and first processor) according to said programmed instructions (See page 10, lines 3-23, and page 10, line 29 through page 11, line 25).

Referring to claim 14, Yeivin teaches the step of re-programming said communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) with instructions (i.e., programmable routines) to enable it to perform transformations of said data stream (i.e., high speed data stream) according to a re-selected communication protocol which is different from the previously selected communication protocol (See page 7, lines 20-22 and page 10, lines 3-23; i.e., wherein in fact that communication processor processes data streams, which are associated with a variety protocols, according to the variety protocols inherently anticipates that said communication handler performs transformations of said data stream according to a re-selected communication protocol which is different from the previously selected communication protocol).

Referring to claim 15, Yeivin teaches the step of generating an electrical signal representing logical bits from a voltage signal having transitions between voltage levels received on said communication bus (See page 9, line 19 through page 10, line 2; i.e., wherein in fact that each peripheral comprises of a state machine which is tailored to at least one communication protocol, and the state machine converts raw data bit stream to a bit stream compatible to a communication protocol inherently

anticipates the step of generating an electrical signal (i.e., communication channel signal) representing logical bits (i.e., bit data) from a voltage signal (i.e., digital communication device signal) having transitions between voltage levels (i.e., digital representation of the communication channel signal) received on said communication bus (i.e., communication channels)) and/or sending a voltage signal (i.e., transmitting said (i.e., digital communication channel signal) having transitions between voltage levels (i.e., digital representation of the communication channel signal) on said communication bus (i.e., communication channels 180 in Fig. 3) generated from an electrical signal (i.e., communication channel signal) representing logical bits (i.e., bit data), according to said communication protocol (See page 7, lines 20-22).

Referring to claim 16, Yeivin teaches the step of decoding/encoding data of said data stream (i.e., in fact, the high speed data stream is encoded/decoded by said communication handler (i.e., peripherals, scheduler and first processor) in a variety of associated communication protocols; See page 10, lines 3-23).

Referring to claim 18, Yeivin teaches the step of identifying and providing as parallel data a data field of logical bits received serially on said communication bus (i.e., communication channels 180 in Fig. 3; See page 9, lines 25-28) and/or providing for sending serially on said communication bus groups of logical bits (i.e., a set of multiple bit words) provided as parallel data (See page 9, lines 28-31).

Referring to claim 19, Yeivin teaches the step of identifying and providing a data frame representing a message from data fields of logical bits (i.e., a set of multiple bit words converted from a received serial data bit stream; See page 9, lines 25-28) and/or identifying and providing fields of logical bits from a data frame representing a message (i.e., a received multiple bit words from the first processor being converted to a stream of single bits to be transmitted into the communication channel; See page 9, lines 28-31).

Referring to claim 20, Yeivin teaches said method is carried out by a communication controller (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) within a microcontroller (i.e., communication controller as indicated by dashed line 119 in Fig. 3).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 3-5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin [WO 00/60477] as applied to claims 1, 2, 6-8, 11-16 and 18-20 above, and further in view of Adams et al. [US 5,761,424 A; hereinafter Adams].

Referring to claims 3 and 4, Yeivin discloses all the limitations of the claims 3 and 4, respectively, including said communication handler (i.e., peripherals 140, scheduler 50 and first processor 90 in Fig. 3) comprises at least one bit engine (e.g., shift register in peripherals; See page 9, lines 26 and 29), which is a bit receiver and/or a bit transmitter (i.e., bit stream receiver/transmitter; See page 9, lines 25-31), except that does not teach said at least one bit engine, which is said bit receiver and/or said bit transmitter, is programmable.

Adams discloses a communication receiver 100 in Fig. 1, wherein at least one bit engine (i.e., packet recognition filter 106 and packet generator parameters 110 in Fig. 1), which is a bit receiver (i.e., packet recognition filter) and/or a bit transmitter (i.e., packet generator parameters), is programmable (See col. 2, lines 5-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined said bit engine (i.e., packet recognition filter and packet generator parameters), as disclosed by Adams, with said at least one bit engine (i.e., shift register in peripherals), as disclosed by Yeivin, for the advantage of providing a programmable recognition filter to determine which received said data streams (i.e., packets) are appropriately to be processed by said communication handler (i.e., receiving node; See Adams, col. 2, lines 2-5).

Referring to claims 5 and 17, Yeivin discloses all the limitations of the claims 5 and 17, respectively, except that does not teach said communication handler comprises a programmable pattern detector, which is performing the step of detecting a predefined pattern in the data of said data stream.

Adams discloses a communication system (Fig. 1), wherein a communication handler (i.e., communication receiver 100 of Fig. 1) comprises a programmable pattern detector (i.e., packet recognition filter 106 of Fig. 1; See col. 4, lines 15-23), which is performing the step of detecting a predefined pattern (i.e., valid information recognized by filter) in the data (e.g., header portion) of a data stream (packets; See col. 3, lines 53-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said programmable pattern detector (i.e., packet recognition filter), as disclosed by Adams, in said communication handler, as discloses by Yeivin, for the advantage of providing flexibility in the update of said communication handler (i.e., receiving node) to recognize new types of said data streams (i.e., packets; See Adams, col. 4, lines 15-17).

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin [WO 00/60477] as applied to claims 1, 2, 6-8, 11-16 and 18-20 above, and further in view of Edwards et al. [US 6,530,047 B1; hereinafter Edwards].

Referring to claim 9, Yeivin discloses all the limitations of the claim 9 except that does not teach a debug unit.

Edwards discloses a system for communicating with an integrated circuit 101 in Fig. 1, wherein said integrated circuit comprising a debug unit (i.e., Debug Circuit 103 of Fig. 1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said debug unit, as disclosed by Edwards, in said communication controller, as discloses by Yeivin, for the advantage of providing a real-time collection of trace information is possible via a high-speed link interface of said debug unit (debug circuit; See Edwards, col. 2, lines 54-62).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeivin [WO 00/60477] as applied to claims 1, 2, 6-8, 11-16 and 18-20 above, and further in view of Sarpangal [US 6,529,970 B1] and Scherpbier et al. [US 6,621,834 B1; hereinafter Scherpbier].

Referring to claim 10, Yeivin discloses all the limitations of the claim 10 including said instructions having been loaded into a memory (i.e., instruction memory bank 130 or first memory bank 70 in Fig. 3) for storing said instructions (See page 10, lines 3-9) to perform transformations of said data stream (i.e., high speed data stream) according to several communication protocols (See page 7, lines 20-22), except that does not teach a peripheral channel connection for rapid loading of said instructions, which perform transformations of said data stream according to custom protocol.

Sarpangal discloses a method and microprocessor with fast program downloading features (See Fig. 1 and Abstract), wherein a peripheral channel connection (i.e., communication medium 7a, dispatcher 5, dispatcher connector interface 5a, and target connector interface 3c in Fig. 1) for rapid loading of instructions (See col. 4, lines 35-62).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said peripheral channel connection (i.e., communication medium, dispatcher, dispatcher connector interface, and target connector interface), as disclosed by Sarpangal, in said communication controller, as disclosed by Yeivin, for the advantage of providing a method of downloading said instructions (i.e., program information) quickly (See Sarpangal, col. 1, lines 66-67).

Yeivin, as modified by Sarpangal, does not expressly teach said instructions perform transformations of said data stream according to custom protocol.

Scherpbier discloses a system and method for voice transmission over network protocols (See Abstract), wherein instructions (i.e., program for communicating in custom protocol) to perform transformations (i.e., enabling transmission/reception) of data stream (e.g., voice data) according to custom protocol (i.e., custom protocol built on top of HTTP; See col. 6, lines 7-8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said custom protocol, as disclosed by Scherpbier, in said instructions, as disclosed by Yeivin, as modified by Sarpangal, for the advantage of providing additional extra information to said communication protocols (i.e., standard HTTP protocol; See Scherpbier, col. 6, lines 8-9).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kelem [US 6,061,417 A] discloses programmable shift register.

Slane [US 6,546,021 B1] discloses method and apparatus for user programmable packet to connection translation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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